Next-Generation IGBTs (CSTBTs)

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Mitsubishi Electric Corporation has announced a carrier stored trench gate bipolar transistor (CSTBT) that has reduced on-state voltages by significant improvements to the carrier distribution in trench IGBTs (TIGBTs). The corporation has developed this CSTBT as its next-generation IGBT. It has demonstrated all of the performance advances hoped for in next-generation power chips. This article describes the results of evaluations of the CSTBT prototypes.

Ever since IGBT modules (used primarily in invertors) were first marketed, new generations of IGBT chips have been produced every few years, steadily improving the performance frontier for the trade-off between switching loss and saturation voltage (an indicator of loss). Until the third generation, improvements resulted from technologies to miniaturize cells, but a revolutionary new structure was introduced in the fourth generation; in addition to further miniaturizing the cells, a trench gate structure was introduced, resulting in a substantial leap in performance.[1]

In response to the needs of a market constantly searching for improvements in energy conservation, the corporation announced its CSTBT in 1996[2], and commenced research and development in both structures and manufacturing processes for these next-generation power chip products.[3]

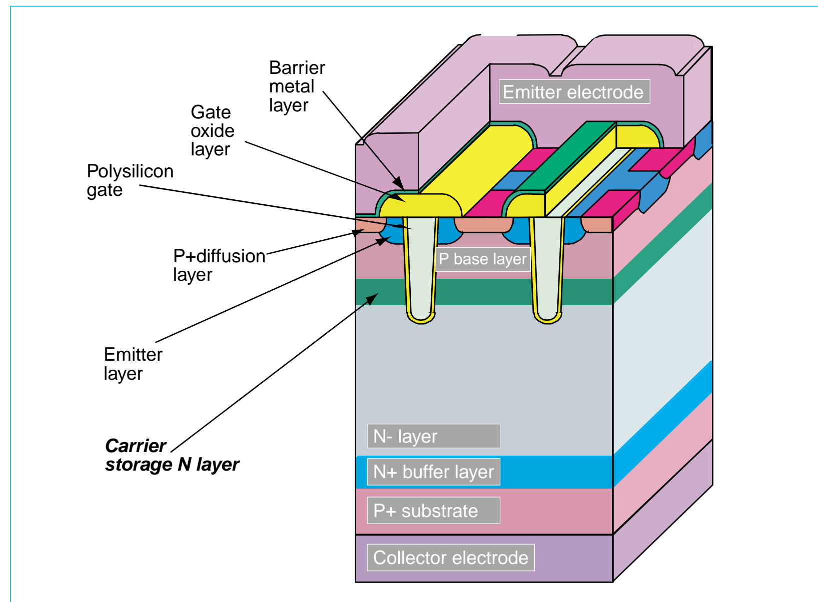

Fig. 1 Three-dimensional view of CSTBT

The Structure and Benefits of CSTBTs

Fig. 1 shows a three-dimensional cross section of a CSTBT. Structurally, the CSTBT is characterized by the addition of an n-type layer with a relatively high impurity density between the p-type base layer and the n- layer in the trench IGBT (TIGBT). When the conventional TIGBT is in an ON state, holes are injected into the n- layer from the p+ layer on the collector side, and these holes pass to the emitter side. On the other hand, in the CSTBT, the impurity density of the n layer that forms a junction with the p base is greater than for the n- layer, so the junction voltage at the junction between the p base and the n layer is greater than the junction voltage at the junction between the p base and the n- layer in the TIGBT. This high junction voltage becomes a barrier preventing the holes that were injected into the n- layer from the p+ layer from passing into the emitter side. In other words, the n layer causes the holes to accumulate within the element by restricting the movement of the holes to the p base layer. This charge accumulation function causes the ON voltage for the CSTBT to be substantially lower than for the TIGBT.

Performance of the 600-volt CSTBT

To confirm the superior properties of the CSTBT, a CSTBT chip was prototyped and evaluated using the same wafers and the same 1μm design rule as for the TIGBT. The CSTBT had a reverse bias voltage of 600V and a current-carrying capacity of 50A. Because, in the CSTBT, the primary junctions were formed with an n-type layer with a relatively high impurity density in order to store the carriers, it was more difficult to ensure reverse-bias voltage capabilities than it

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was for the TIGBT; however, the reverse bias voltage was successfully secured by optimizing both the thickness and the impurity density of the carrier storage layer, and by using high precision control. Fig. 2 shows the waveforms for the current and the voltage when the CSTBT is OFF. As is clear from the figure, the CSTBT rated at 600V has a 720V reverse bias capability, so there is adequate margin above the rated voltage.

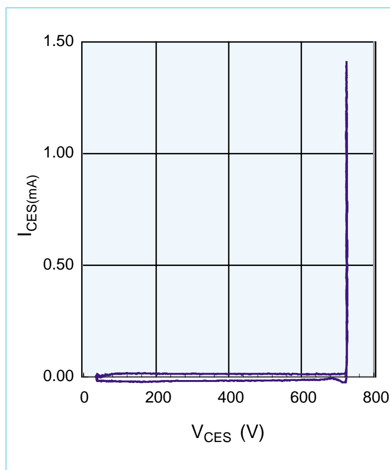

Fig. 2 Breakdown voltage of CSTBT.

Fig. 3 shows the output characteristics of a CSTBT exposed to electron-beam radiation in the same way as a TIGBT is exposed (in order to control the minority carrier lifetime). The output characteristics are shown at both 25°C and 125°C. The

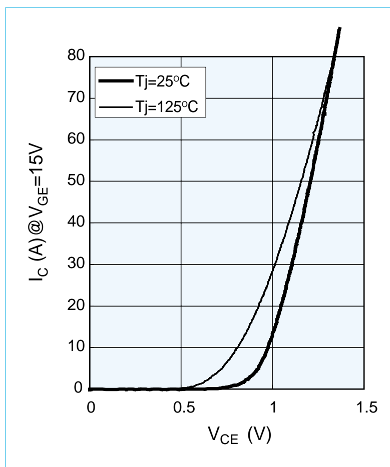

Fig. 3 I-V characteristics of CSTBT.

saturation voltage at the rated current ($V_{CE(sat)}$) was 1.22V at T_J=25°C, and 1.15V at T_J=125°C, 0.3 to 0.4V less than the conventional TIGBT.

Fig. 4 is a curve showing the tradeoffs between the switch-off loss, $E_{SW(off)}$ and the $V_{CE(sat)}$. As described above, the CSTBT is superior to the TIBGT in terms of its ON characteristics, and thus the CSTBT tradeoff curve is about 0.4V better than the TIGBT for the same switching loss. When it comes to this tradeoff relationship between the $V_{CE(sat)}$ and the $E_{SW(off)}$ the CSTBT is superior to any other MOS gate device so far announced for applications at 600V.

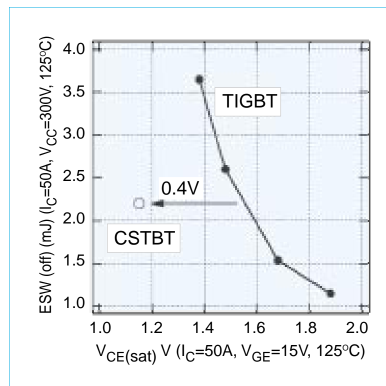

Fig. 4 Trade-off relationship between on-state voltage drop and turn-off loss for both CSTBT and TIGBT.

It was also confirmed that the reverse bias safe operation area (RBSOA) could perform turn-off switching at 500A (a current density of 2100A/cm^2), ten times the rated current.

As described above, the CSTBT proposed by Mitsubishi Electric is positioned as the next-generation power chip after the TIGBT, and, as a step in this direction, the corporation has developed technologies for insuring reverse biasing capabilities and has established design technologies for carrier storage layers, validating the performance of the 600V/50A CSTBT. As a result, the CSTBT has been able to improve the tradeoff relationship between the $V_{CE(sat)}$ and the E_{OFF} by about 0.4V over the conventional TIGBTs without incurring any loss in performance in terms of the switching time or reverse bias voltage. This tradeoff relationship is the best of any MOS gate element announced to date for 600V or above.

Development efforts are underway on high-performance module products using the CSTBT chips in order to contribute to the market looking for improved energy conservation. ❑

References

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